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A 14 GHZ DELAY LOCKED LOOP WITH MINIMIZED PERIOD DELAY ERROR AND  
WORST 1.5% DUTY CYCLE ERROR

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**Gegham Petrosyan**

PhD in Technical Sciences

YSU, Electronics, Micro and Nano Electronics

[geghamp@synopsys.com](mailto:geghamp@synopsys.com)

**Albert Gevorgyan**

PhD student

NPUA, Microelectronic Circuits and Systems Interfaculty

[galbert@synopsys.com](mailto:galbert@synopsys.com)

**Lyudvig Hakobyan**

PhD student

NPUA, Microelectronic Circuits and Systems Interfaculty

[lyudvig@synopsys.com](mailto:lyudvig@synopsys.com)

**Sargis Ghulyan**

Bachelor student

YSU, faculty of Radiophysics

[ghulyan@sunopsys.com](mailto:ghulyan@sunopsys.com)

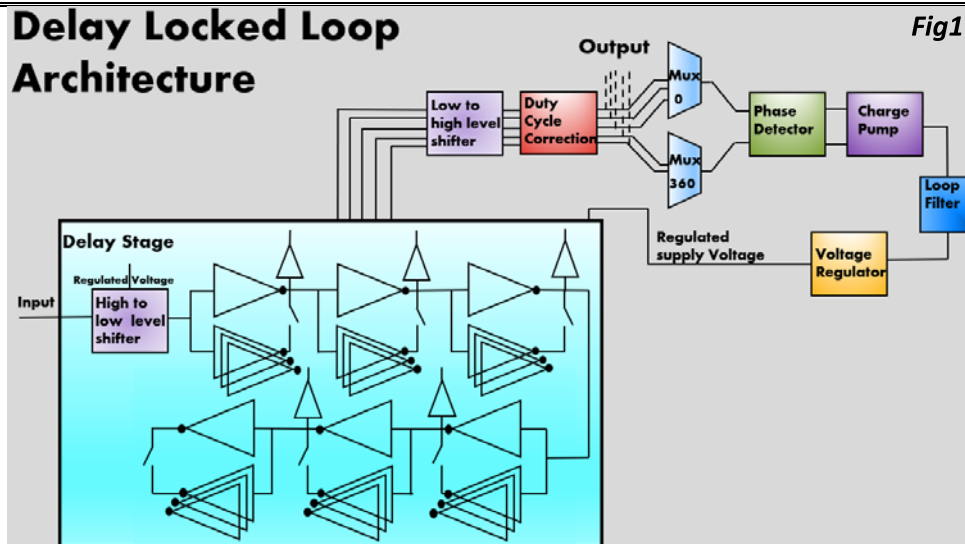
**Abstract**

In many applications, the Delay Locked Loop (DLL) is used to improve the timing margin for better performance of the synchronous system. A precise 50% duty ratio of the clock signal is essential to the DDR SDRAM, which needs both the rising edge and the falling edge of the clock to sample the data. The duty mismatch of the output clock in the DLL may be caused by the duty error of the external input clock or by the common mode voltage offset in the voltage-controlled delay line (VCDL). Many studies have presented the duty cycle corrector (DCC) to reduce the duty mismatch of the clock. This paper proposes a high-frequency DLL that generates multiphase clocks with a wide frequency range. The object of this research is to have  $\pm 1.5\%$  duty cycle error at the output clock and, in locked state, less than 2% of clock period delay between 0- and 360-degree phases (delay error). This generator produces 8 phases at 14 GHz.

**Keywords:** delay locked loop, phase frequency detector, charge-pump and loop filter, inverter, duty cycle.

**Introduction**

Delay locked loops (DLL) and Phase locked loops (PLL) have become important components for valid data transmission in high-speed interface systems, frequency synthesizers, clock and data recovery circuits, transceivers [Kuo-Hsing Cheng et al.] and wireless systems [Chua-Chin Wang et al.]. In order to have high frequency clock signals in SERDES design PLL is used [Loke et al.]. For having multiple phases in PHY we use DLL [Ranjan, Anurag]. DLL usually takes reference clock from PLL. For DLL lock range, lock time, duty cycle of output clock, delay error in locked state and power are key parameters. Conventional DLL consists of a voltage-controlled delay line (VCDL), phase frequency detector (PFD) [Khare et al.], charge pump (CP) and loop filter (LF).



Architecture of DLL

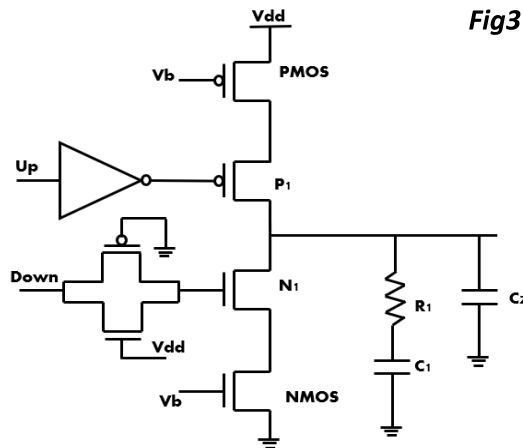
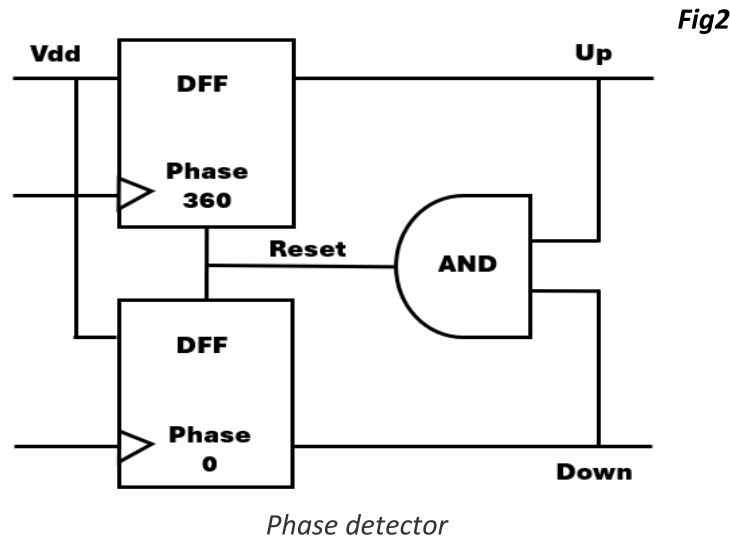
In the designed DLL in the locked state, two circuits are used to ensure that the duty cycle is correct and that the delay error is as small as possible. The first is known as DCC circuit, and the second is known as the voltage regulator (VREG). In the locked state, two circuits are used to ensure that the duty cycle is correct and that the delay error is as small as possible. The block diagram of designed DLL is shown in Fig 1.

The section II introduces the structure of the DCC proposed circuit, and it's transient analysis. The section III discusses observed results of related circuits.

## II Architecture

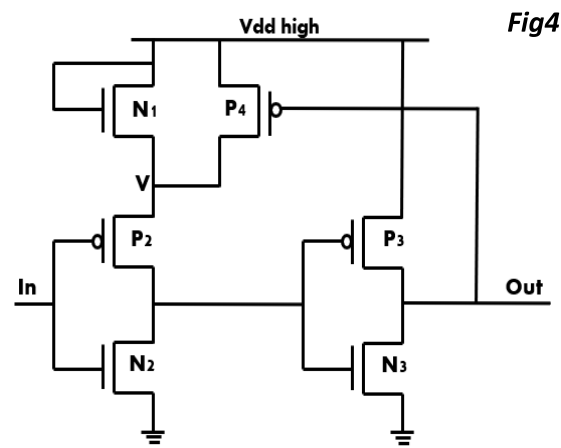
### PFD

The PFD circuit design, given in Fig.2. The main function of PFD is measuring the phase difference between reference clock (Phase 0) and the VCDL output clock (Phase 360) and generating the output signals containing phase error information. The phase error information is given by Up and Down PFD output signals. PFD is designed by two D flip-flops (DFF) and AND gate. The Ref and VCDL output clocks pass through DFF's clock input, and the 'D' input is set to Vdd. The outputs pass through the AND gate which reset them. The PFD with flip-flop configuration DLL locking is faster than others because it can detect both phase differences.



Charge Pump and Loop filter

Fig3



Low to High level shifter

Fig4

**CP and LF**

The CP and LF designs are given in Fig.3. The CP consists of current sources (NMOS and PMOS), switch transistors N1 and P1, Inverter and TG gate. The action of CP is taking the Up and Down signals going from PFD in the form of voltage pulses and convert to current by opening N1 and P1 switches. As long as the UP signal is high, the P1 switch opens and PMOS current source charges the loop filter. The N1 switch opens and NMOS current source discharges the loop filter capacitor C2 while Down signal is high. NMOS and PMOS transistors dimensions must be adjusted to provide same current for same input voltage. The TG gate have same delay as Inverter. Loop Filter is a series connection of C1 capacitor and R1 resistor and parallel C2.

**Low to High Level shifter.**

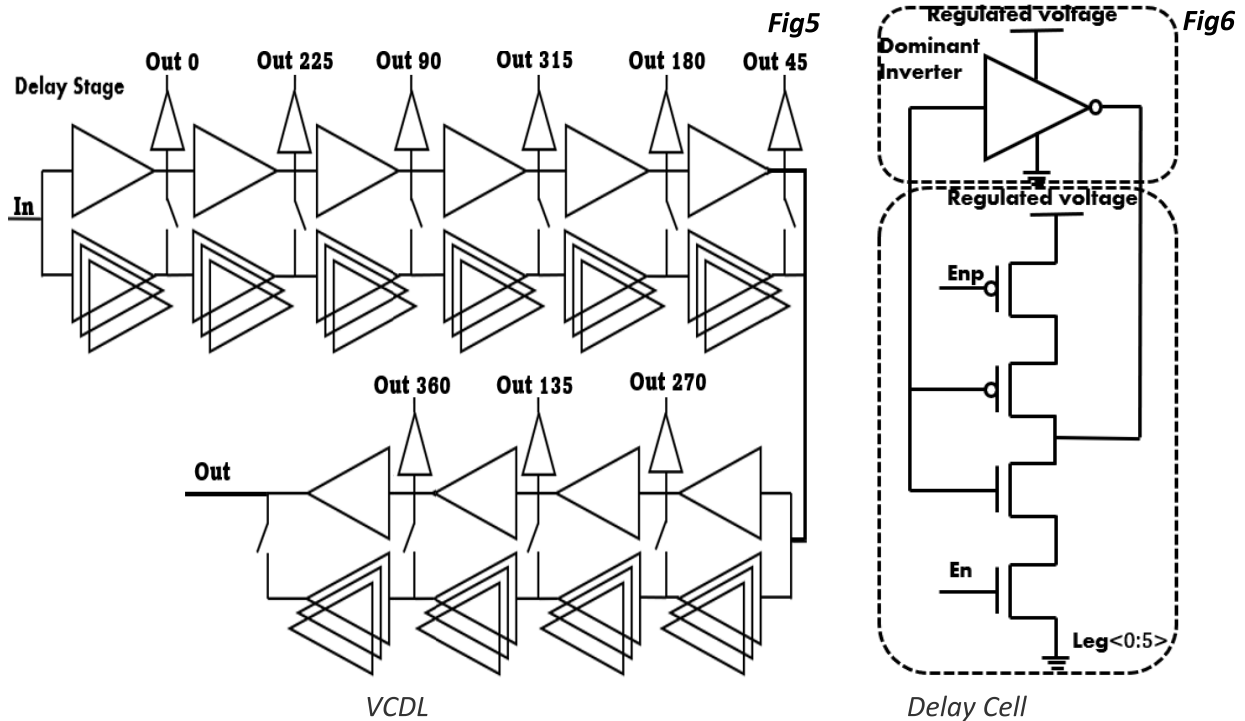
Low to high level shifters are used to restore clock's high voltage level after VCDL. The level shifter is designed by simply reducing the supply voltage of inverter P2-N2 by addition of a diode connected nmos N1 device. The voltage at node 'V' is defines by following expression [1].

$$V = V_{dd} - V_{thN} \quad [1].$$

which reduces gate-source voltage of P2 to turn it OFF when 'in' is HIGH. When 'in' is LOW, the feedback transistor P4 turns ON thereby charging node v to Vdd high. This is required in order to turn the transistor P3 completely OFF as it is operating on Vdd high supply level.

**VCDL**

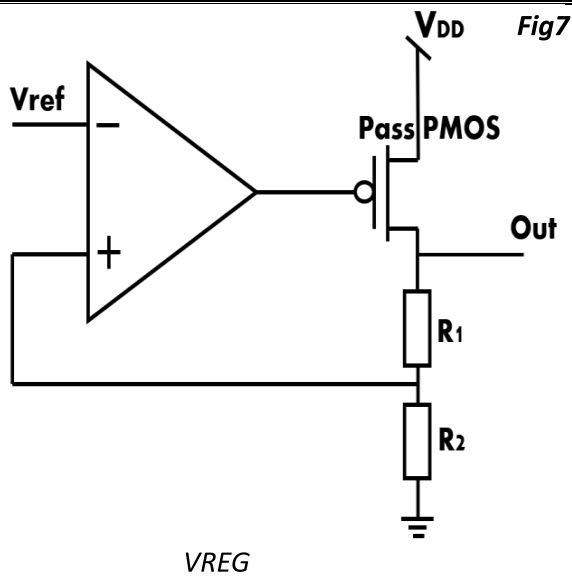
The VCDL circuit design is given in Fig.5. In this paper VCDL is designed for 8 output phase generation. The VCDL constructed by 10 delay cells, the last one is used as dummy for 9<sup>th</sup> cell to have the same load as others. Each delay cell delays the input clock 225 degree. At the output of each delay cell a buffer is used. The main function of VCDL is to take the reference clock signal and by using delay cells delay it to have exactly one clock period time on the last output phase of the DLL. The delay should be controlled with their supply voltage coming from the VREG which is defined by the feedback loop. Delay cells consist of one dominant inverter and 6 parallel connected three state inverters (Legs). By increasing number of working Legs, we increase the current causing the delay between legs decrease and vice versa. The voltage taken from LF is used as supply voltage for delay cells. The feedback loop controls the whole system and adjust the amount of delay and the voltage coming from VREG. Delay depends on the voltage applied to delay cells. The greater supply voltage leads to greater switching current of delay cells eventually the smaller delay between phases is obtained. The delay cell design given by Fig.6.



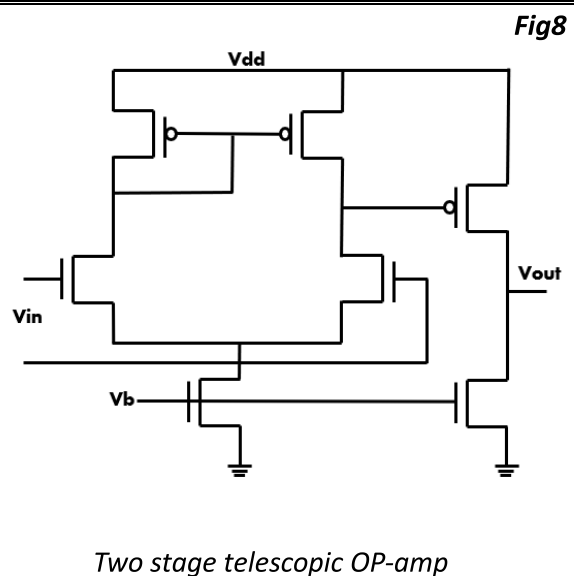
**VREG**

The VREG circuit design, given in Fig.7. The Voltage Regulator is designed on two stage operation amplifier, output PMOS pass transistor and feedback resistors. The VREG repeats the voltage from the LF into the VCDL. LDO VREG achieves a stable regulated output voltage during the line regulation and load regulations. The two-stage op-amp provided big open loop gain and stable feedback network. The dimensions of pass transistor should be very high to provide a large current. Pass transistor is chosen PMOS which will provide large output voltage swing. All transistor's sizes (W-width, L-length, nfin-number of fins, nf-number of fingers and m-multiple) optimized to keep them in saturation region. We change and tweak the resistor value using the given formula [2].

$$V_{out} = V_{ref} \cdot \left( \frac{R1}{R2} + 1 \right) \quad [2].$$



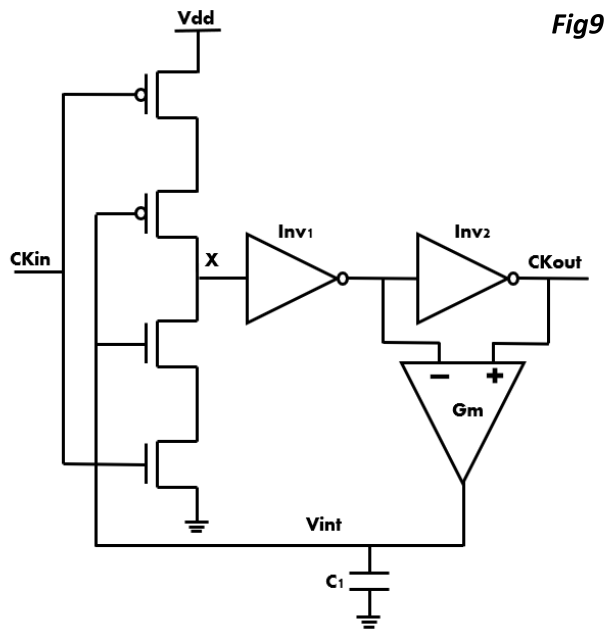
VREG



Two stage telescopic OP-amp

**DCC**

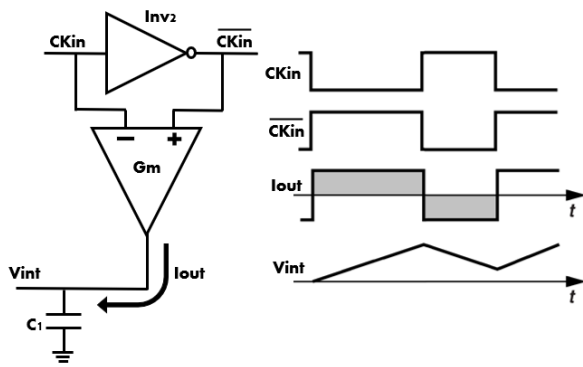
The DCC circuit design is given in Fig.9. DCC scheme implemented in two parts [Eunseok et al.]. The first part operation is measuring the time difference between high and low voltage times clock in same period.



Duty Cycle Correction circuit architecture

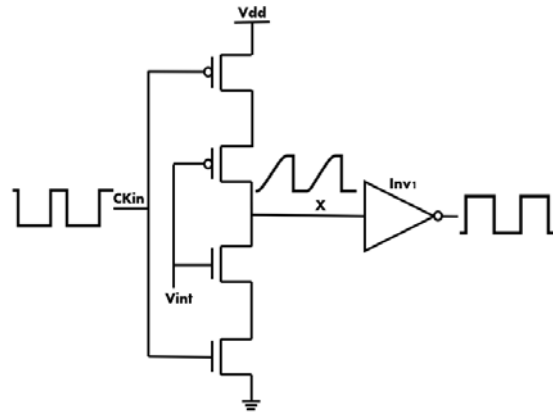
Second part of the circuit should adjust the duty cycle of the clock. Here, when CKin is low, the Gm stage charges C1 and vice versa. Thus, if  $\Delta T \neq 0$ , the average value of Vint continues to rise (or fall), serving as a measure of the duty cycle error. When input is low, M3 slows down the rising edge in output. Similarly, M4 controls the falling edge. The second inverter sharpens the transitions and produces a duty cycle that depends on the rise and fall times at 'X'. In this paper telescopic Op-Amp architecture is used. The duty cycle error measuring scheme is given by Fig.10. The duty cycle adjustment scheme is given by Fig.11.

Fig10



Duty cycle error measuring scheme

Fig11



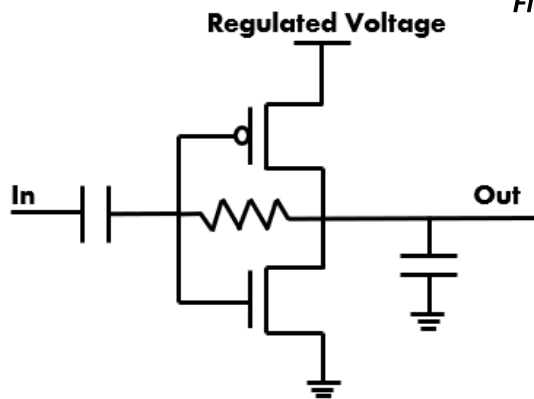
Duty cycle adjustment scheme

**Additional Building Blocks to finish the DLL.**

**The input level shifter and multiplexer**

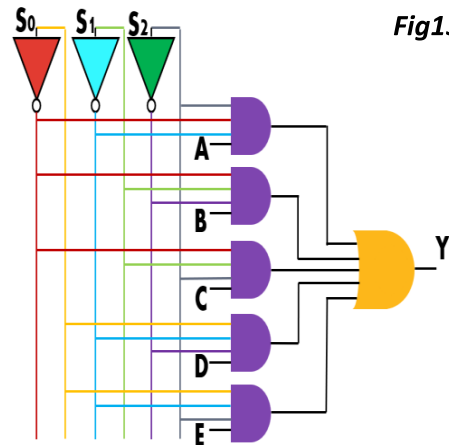
Multiplexer (Fig.13) is used for selecting 0 and 360 degrees from all phases. At the input ac coupling high to low level shifter is used for converting input clock's high voltage level to VREG output voltage. High to Low ac coupling level shifter is a linear amplifier with input ac coupling cap. Circuit diagram and output function given by Fig12.

Fig12



Input Ac coupled level shifter

Fig13



Multiplexer

**III Simulation Results**

**VCDL**

Because input frequency 14GHz and VCDL designed for 8 output phases each delay cell must delay clock  $71.4/8=8.9$  ps delay. Shown in below table (Fig.14) is measuring delay of delay cell for VDD and Vdd/2 supply voltages. For FF case we must close min 5 of 6 legs for having 8.9ps delay.

Fig14

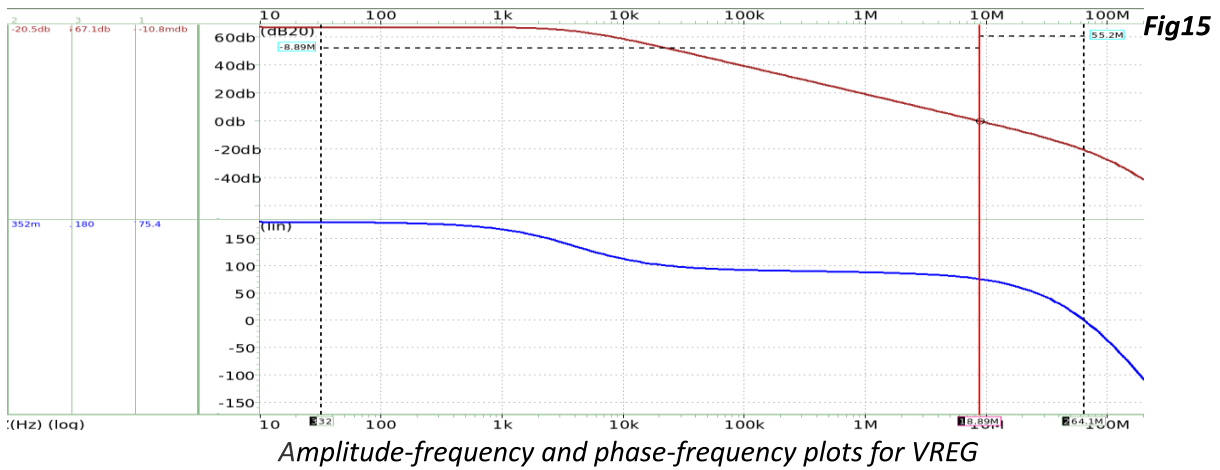
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	Supply voltage $V_{dd} = 0.9v$			Supply voltage $V_{dd}/2 = 0.45v$		
Number of Open legs	Delay time TT ps	Delay time FF ps	Delay time SS ps	Delay time TT ps	Delay time FF ps	Delay time SS ps
6	4.4	4	4.8	9	12.5	6
5	4.7	4.4	5	9.5	12.7	6.6
4	5	4.8	5.3	10	12.9	7.3
3	5.5	5.3	5.6	10.4	13.1	8.1
2	6	5.9	6	10.7	13.2	9.1
1	6.5	6.6	6.4	11.1	13.4	10

*Delay with changing leg count*

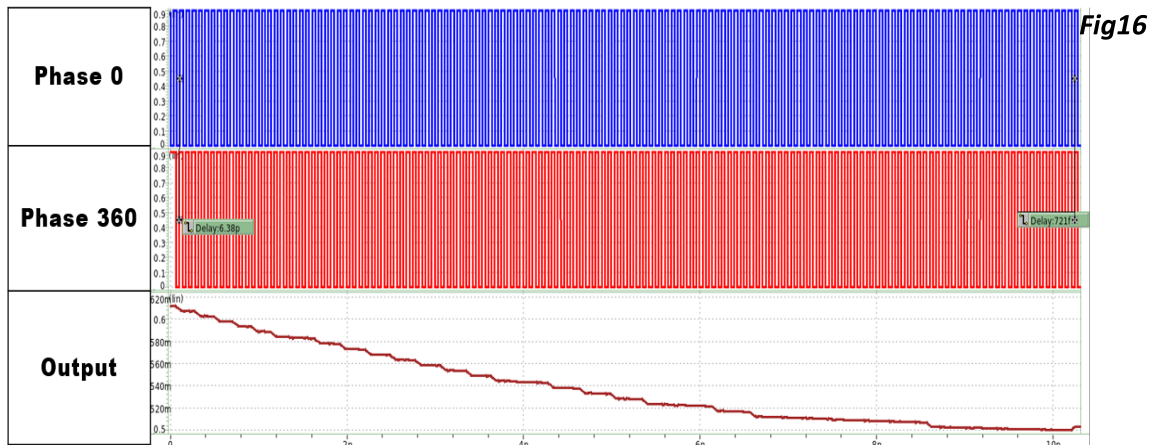
### VREG

Running Ac simulations for 2 stage Op-amp. Results shown in Fig .15. All transistors are in saturation region. The input voltage is 500mv. For VREG measured DC gain – 67.1 dB, Phase margin – 75, Gain margin – 20.5dB.



### PFD CP and Loop Filter

The delay error 721fs.



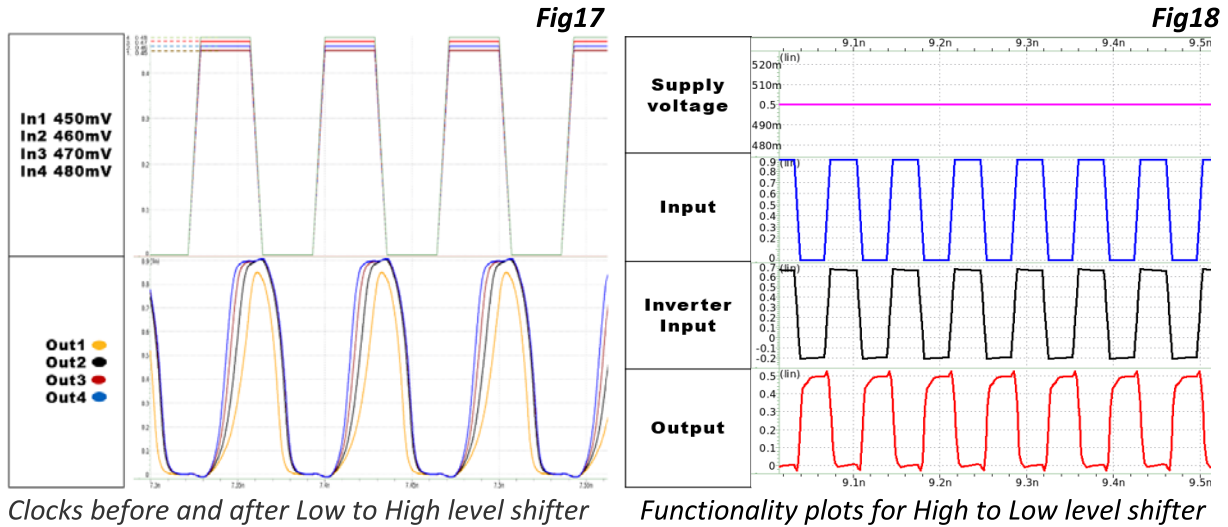
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### Delay error and PFD output voltage

#### **Low to High level shifter and input ac coupling High to Low level shifter**

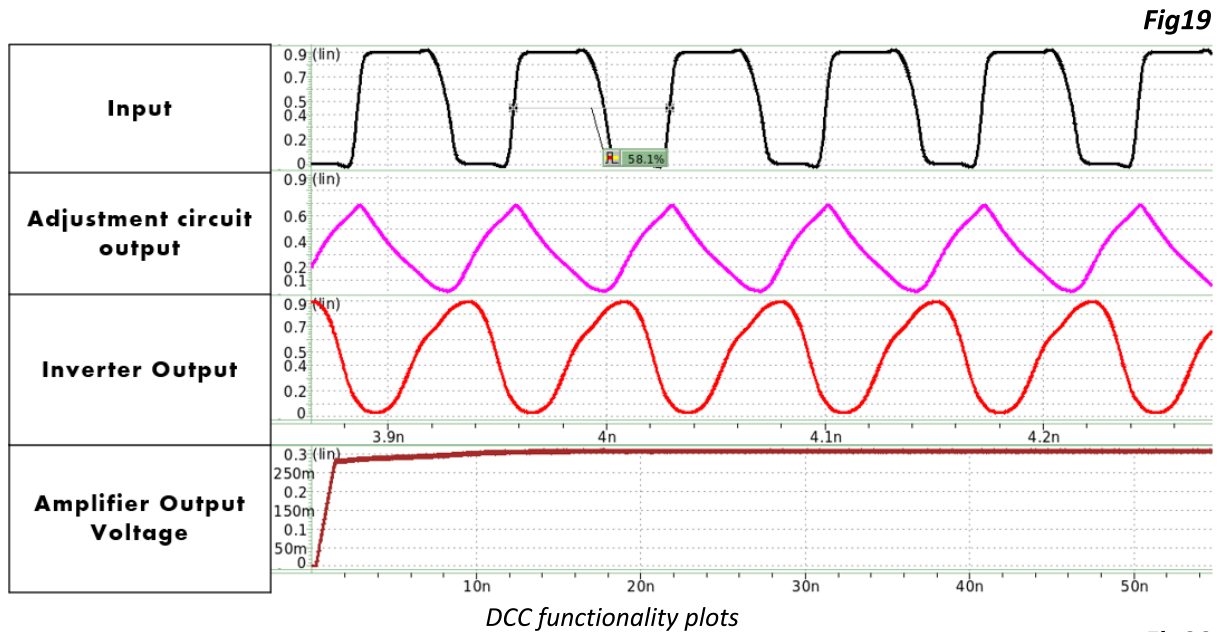
If input clock signal's voltage high level grater than 460mv the output will be Vdd(900mv). The waveforms for these measurements are shown in Fig.17.

Shift input signal high voltage level from Vdd (0.9v) to 0.5v. The circuit functionality waveforms are shown in Fig.18.



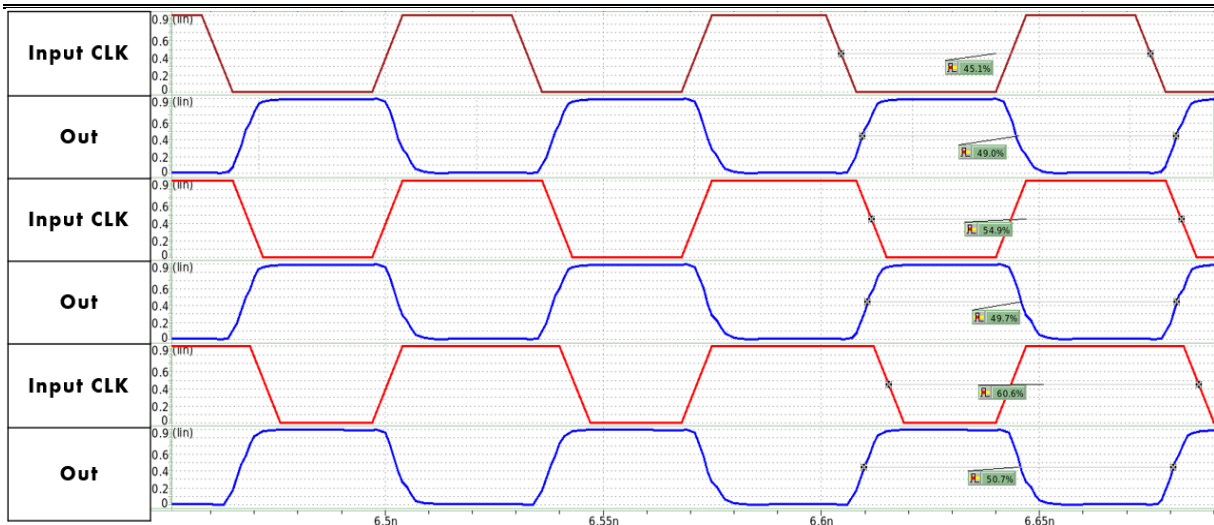
#### **DCC**

For evaluate circuit functionality running transient simulation with different input clock duty cycle. The waveforms for these measurements are shown in Fig.19. In input 14GHz clock. Second simulation for fix how circuit works with different duty cycle. Sweep duty cycle 35%-45%. The waveforms are shown in Fig.20



**Fig20**

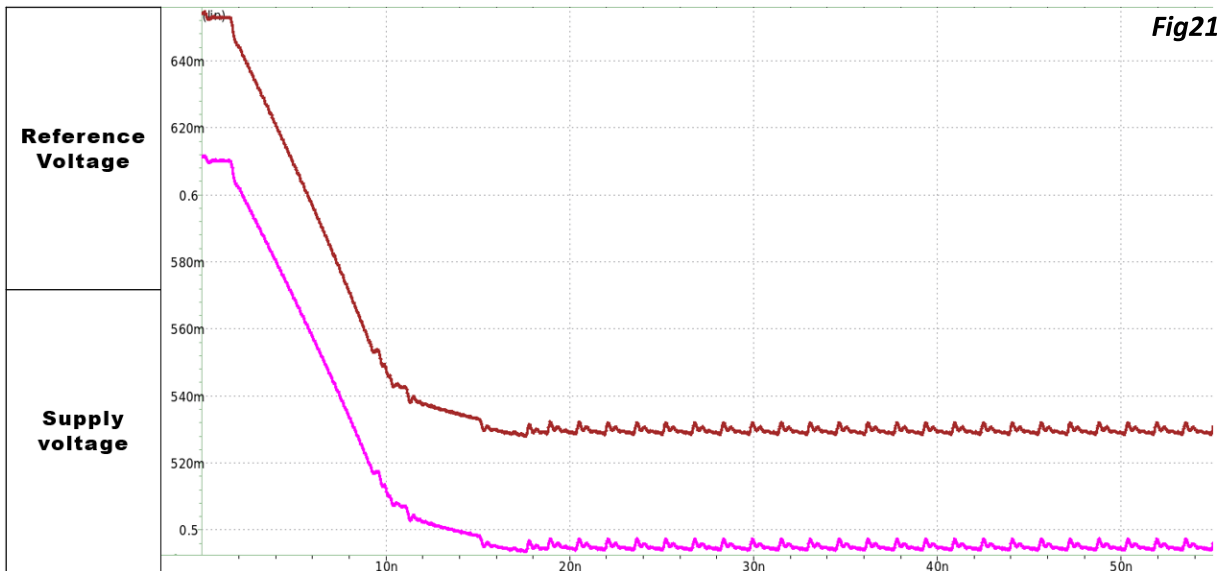
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*Input and output plots of the DCC*

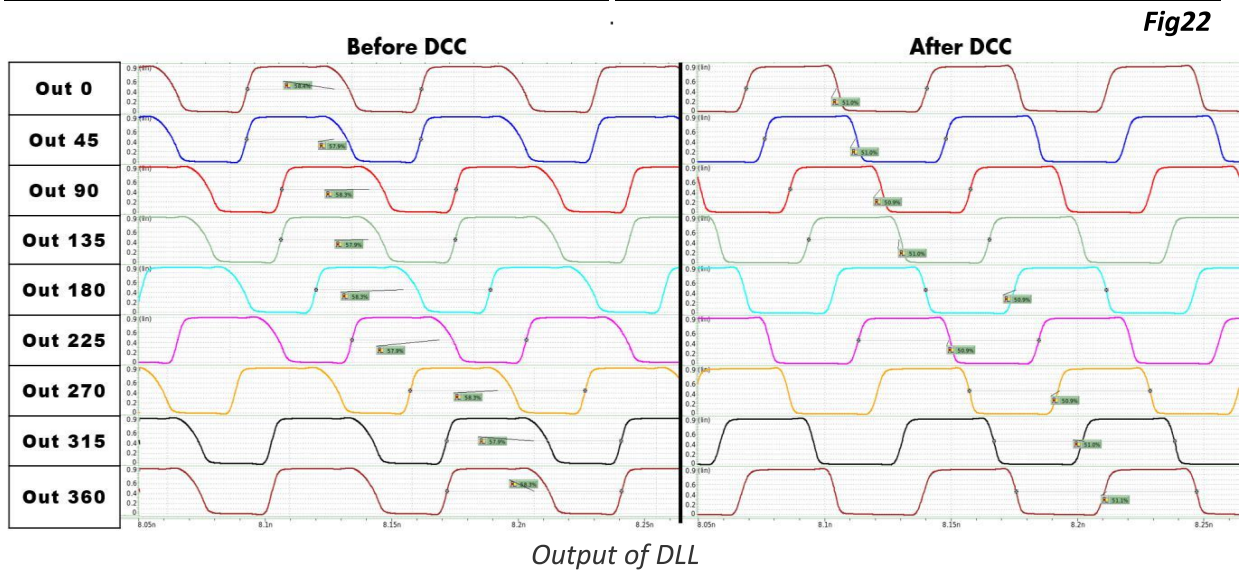
### ***Top-Level simulations***

Running top level simulations with 5 close legs,  $R1 = 700\text{m}$  and  $R2 = 10000\text{m}$  conditions. Measures the regulated supply voltage for VCDL and Reference voltage of VREG. The waveforms given by Fig.21. In Fig.22 shown output 8 clock before and after DCC when DLL is locked. The duty cycle and frequency measurement for each clock are shown in Fig.23.



**Fig21**

*Regulated supply voltage for VCDL and Reference voltage of VREG.*



**Fig23**

	Ph 0	Ph 45	Ph 90	Ph 135	Ph 180	Ph 225	Ph 270	Ph 315	Ph 360
Duty cycle In %	51.056	51.03	51.032	51.014	50.099	51.612	50.981	51.582	51.043
Frequency In GHz	13.999	13.993	14.004	13.994	13.993	14.001	14.003	13.999	14.031

*Duty cycle and frequency*

**IV Conclusion**

In this paper besides the traditional DLL scheme, other schemes were also added. DCC for correct duty cycle of output clock and VREG for minimize the delay error. For having better correction and wide delay range in VCDL developed by adding delay legs. The simulation results show that in 14 GHz output clocks looked better than in previous DLLs. The measurements show that DLL locked with 721fs delay error, worst 51% duty cycle.

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