OUTPUT FREQUENCY STABILIZING OF THE CMOS RING OSCILLATOR

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Abstract

Nowadays there are many concerns while designing IC-s (Integrated Circuits) (integrating circuits) such as power consumption, the area, the speed, the noise and the other effects arising from the ones mentioned. One of the main drawbacks of CMOS ring oscillators used for generating clock signals in modern IC's is the jitter on its output frequency. It may occur due to variation of the ring oscillator's supply voltage, which is mainly caused by noise. In this paper the circuit proposed for decreasing the noise on supply voltage of the ring oscillator. As a result the jitter or the phase noise of its output frequency is decreased.

The reference voltage source with -90dB PSRR and with the 2mV change on its output voltage for -40...125 temperature change, the low-pass filter and the voltage regulator with -74dB DC PSRR are used for stabilizing the supply voltage. This combination reduces the output frequency change of the ring oscillator from ±2GHz for nominal 10GHz frequency to ±65MHz for low frequency supply noise and to ±23MHz in case of high frequency supply noise.

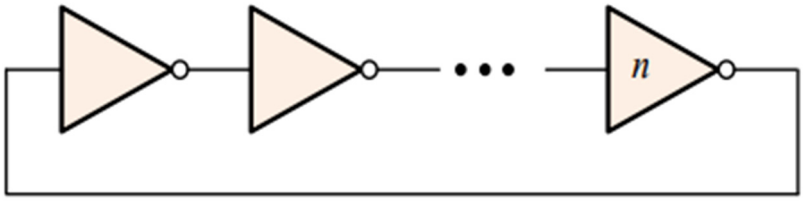
Keywords: ring oscillator, Op-Amp, inverter, output frequency, supply noise, offset.

Introduction

Since the modern digital circuits mostly are sequential synchronized systems, clock pulse signals are used for transmitting, receiving, and processing data. These signals are generated by special circuits called oscillators. Ring oscillators are widely used in phase-locked-loops (PLL) for clock-data recovery, frequency synthesis, clock synchronization in microprocessors and many other applications [Weigandt et al.].

Usually ring oscillators are used for generating clock signal which consists of cascade connected odd numbers (minimum 3) of inverters in a feedback loop.

Fig. 1



Ring oscillator consisting of N inverters

Each inverting stage in the ring contributes a time delay to the total period of oscillation [Pialis, Phang]. The output frequency (F_{out}) depends on N number of inverters and the delay time of each inverter (Td).

$$F_{out} = 1/N * T_D \qquad (1)$$

The inverters should be identical to avoid possible inaccuracies. The equation (1) shows that the oscillator frequency can change according to any change in TD. Irregular changes in Td are causing inaccuracies during transmitting, receiving or processing data. To avoid them it needs to consider the parameters defining TD mentioned in equation (2).

$$T_D = 0.7 * R_p * C + 0.7 * R_n * C \qquad (2)$$

Where the Rn and Rp values are the resistances modeled accordingly for NMOS and PMOS transistors, C is the output load for each inverter.

Slowing inverters by extra capacitors or RC filters allows to decrease the count of the inverters by slowing their transient response (increasing inverter delay TD).

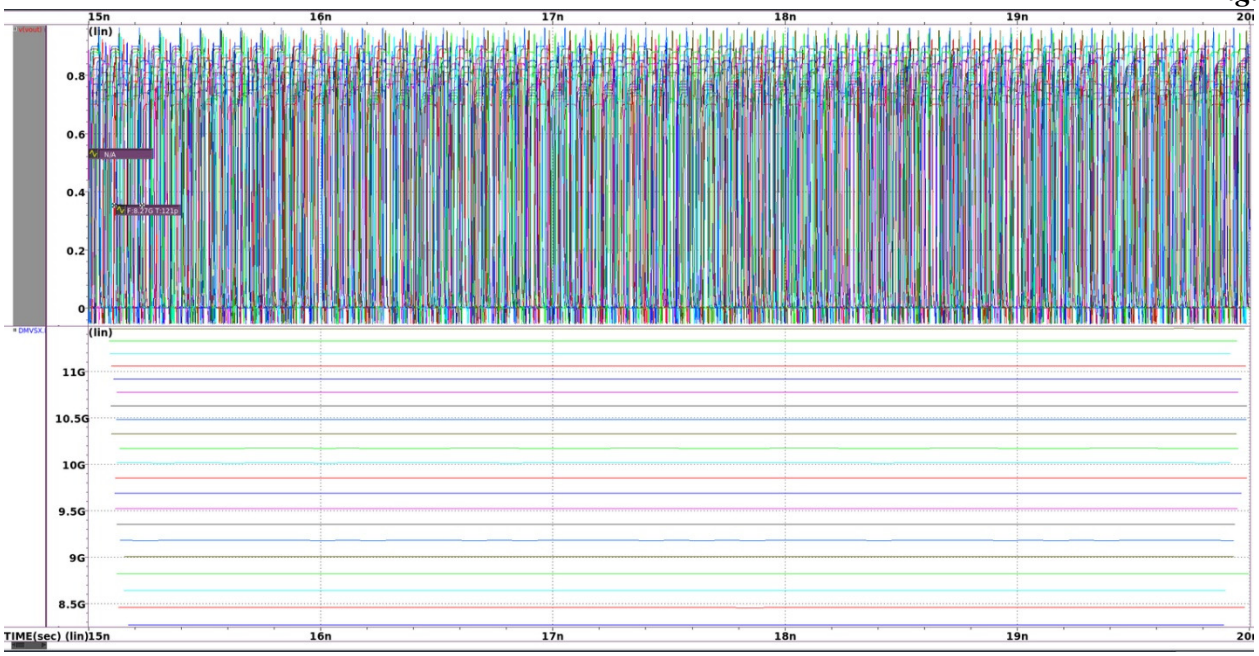
As modern IC-s work frequencies can reach to several GHz-s even a small-time change in the clock signal can cause noticeable deviations. The stability of the ring oscillator output frequency is naturally affected by its supply voltage, temperature and process parameters variations.

Problem description

As supply voltage changes impact is linear on RO's output frequency the supply noise will change the output frequency causing jitter. This type of jitter is called deterministic jitter (DJ). To minimize DJ, we need to increase stability of the supply voltage. The external voltage sources usually have ±10% variation rage.

To show the dependence of the RO's output frequency on its supply voltage the simulation is done for 14nm FinFet technology. The supply voltage is swept in 700-900mV range with 10mV step. As we see in Fig. 2 the output frequency is varying in 8-12GHz range.

Fig. 2

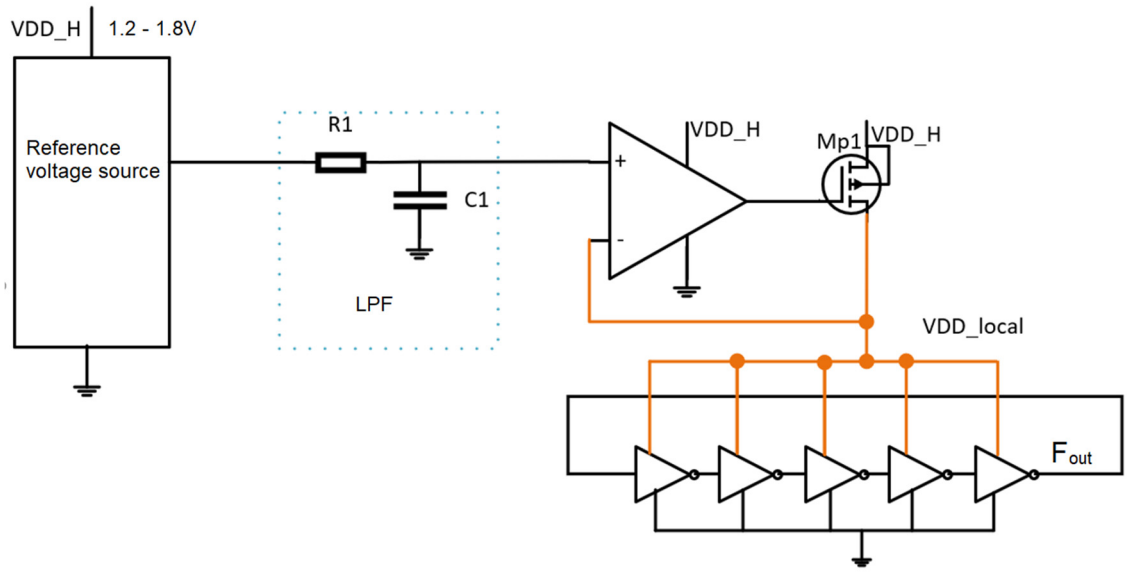


RO's output frequency variation caused by changing supply voltage

Proposed solution

For stabilizing supply voltage a special circuit is used consisting of three main nodes. The main idea is to use a circuit which provides reference voltage with ±1% stability. Its supply voltage is 1.2-1.8V. The circuit inside the reference voltage source allows us to keep the mentioned stability value regardless to the environment temperature, tech process or the change on the supply voltage. Minimizing the impacts of thermal and other types of noise in the basic inverter cells attenuates the jitter [Weigandt et al.]. After the main circuit the low-pass filter (LPF) is placed to filter the high-frequency components on the reference voltage. This allows us to give a noiseless reference voltage with higher stability to the third node which is the Op-Amp in the feedback loop (voltage regulator) which stabilizes the RO's supply voltage (Fig 3).

Fig. 3

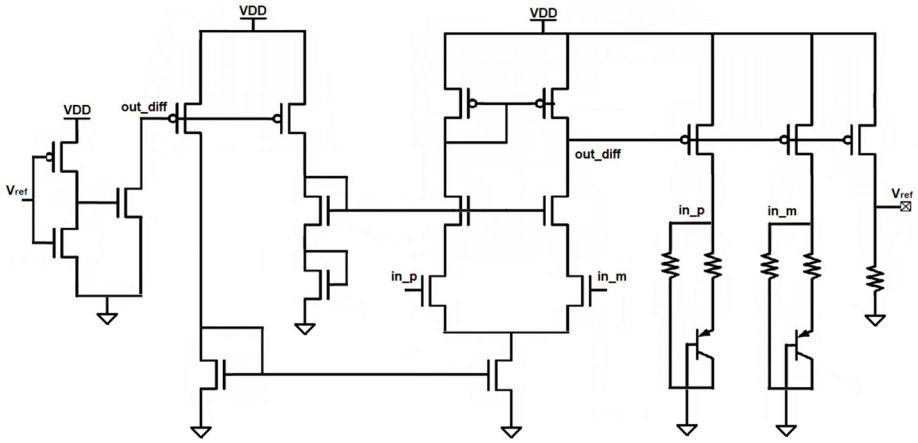


The proposed circuit stabilizing RO's supply voltage

The Op-Amp's stability coefficient depends on its input offset. To minimize the offset Op-Amp needs to have high gain (Av): particularly for 0.8V reference voltage we need Av to be 1000 (60dB) to obtain 0.8mV offset. The multi cascade Op-Amp structure is used having common-source with input PMOS transistor as output stage.

The bandgap reference circuit is designed to produce a stable and precise output reference voltage which is independent of variations in PVT [Akshaya, Siva] (process, voltage, temperature) and used circuit for reference voltage source. It consists of a Diff-Amp and the output stage (Fig. 4).

Fig. 4

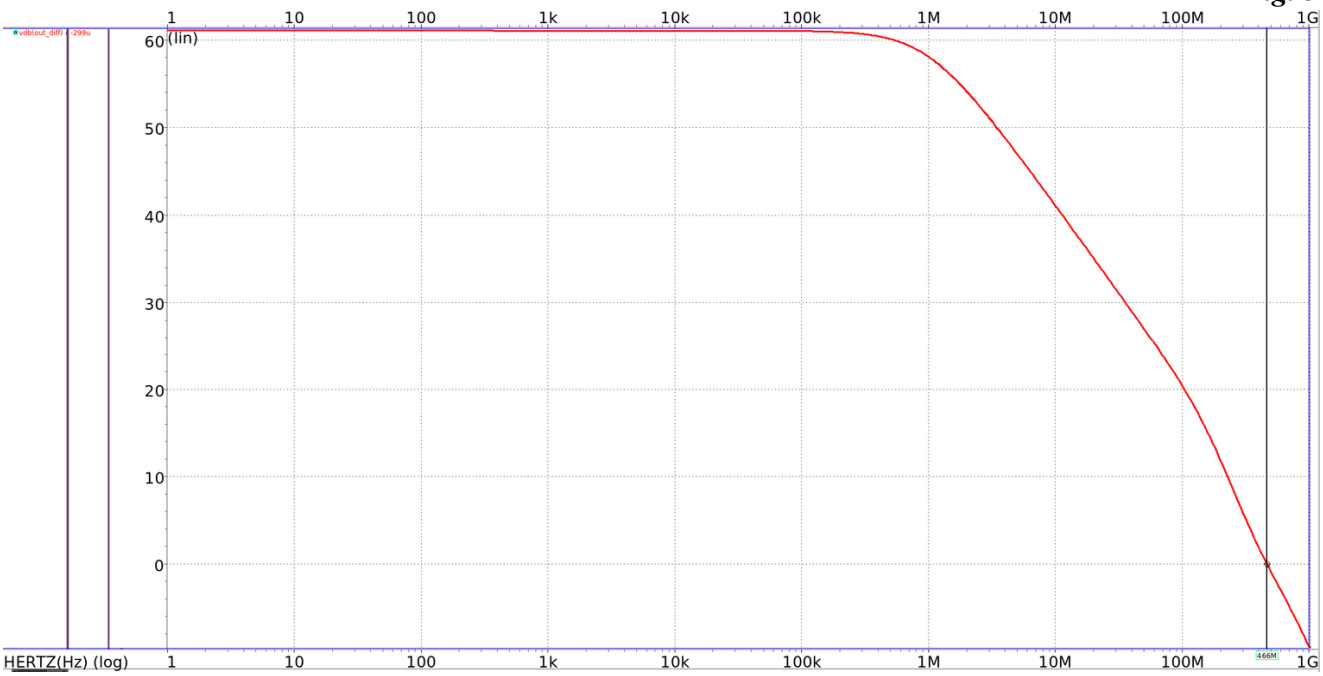


The circuit inside reference voltage source

For proper biasing the power-on node is added to the circuit. It opens all the PMOS transistors in the system, while the Vref will reach the value to switch the CMOS inverter and turn off the NMOS transistor.

For Diff-Amp 60dB DC gain is obtained with 460MHz cut-off frequency (Fig. 5).

Fig. 5



The amplitude-frequency plot for Diff-Amp

Multiple verifications are done for the system such as transient, phase-frequency, PSRR, thermal dependence analyzes.

For whole system the following results are measured:

- DC gain – 66dB
- Phase margin – 94°
- Gain margin – 26.4dB
- PSRR DC value is -90db
- Max PSRR value is -3.31dB at 270MHz
- 2mV change on V_{ref} for -40...125 temperature change
- 40mV change on V_{ref} for 1.5-2V supply voltage change

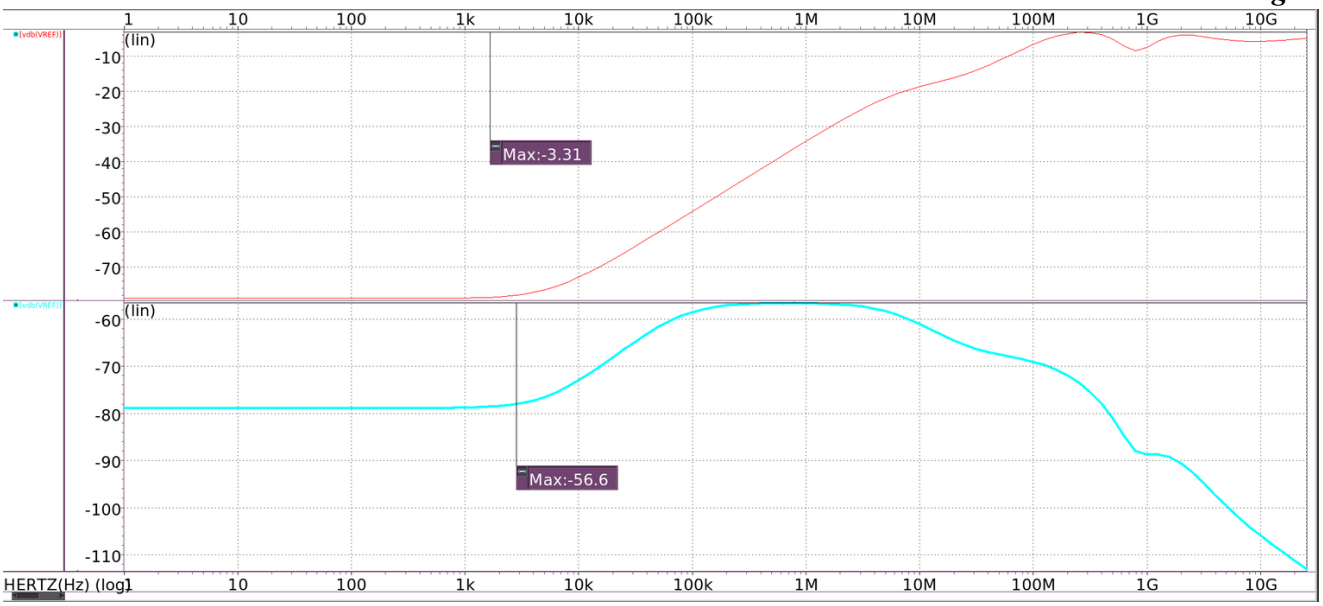
As started from 10MHz PSRR is higher than -20dB we need the LPF to suppress noises with mentioned and higher frequencies. So, the LPF with 100KHz cut-off frequency (fc) is placed after reference voltage source taking into account possible process deviations. The value of resistance is picked 100KΩ, so from equations 3.1 and 3.2 the capacitance value is equal to 15.92pF:

$$f_c = \frac{1}{2*\pi*R*C} = 100KHz \qquad (3.1)$$

$$C = \frac{1}{2*\pi*100K*100K} = 15.92pF \qquad (3.2)$$

For comparing the PSRR results for connecting reference voltage source and LPF in series with previous results the same measurement has been done.

Fig. 6



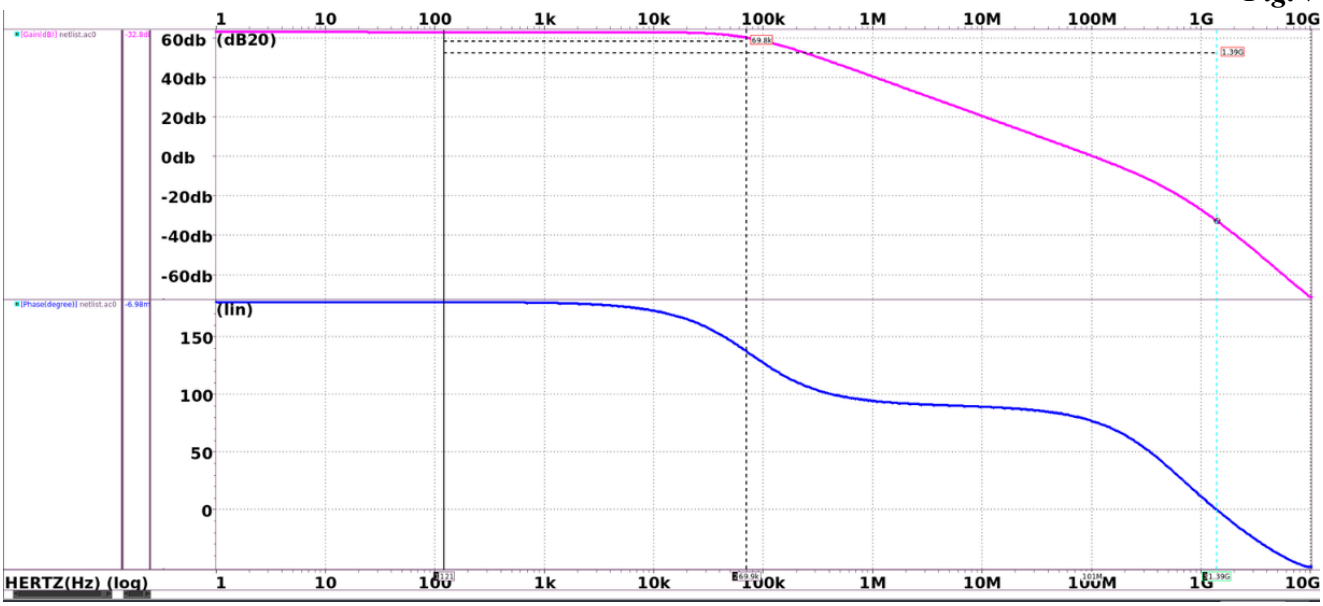
PSRR plots for reference voltage source without and with LPF

As we can see from Fig. 6 the maximum PSRR value is decreased from -3.33dB to -56.5dB. After optimization the following parameters are measured for the voltage regulator:

- DC gain – 63dB
- Phase margin – 76^{o}
- Gain margin – 33dB
- DC PSRR – -75dB
- Max PSRR – -23dB

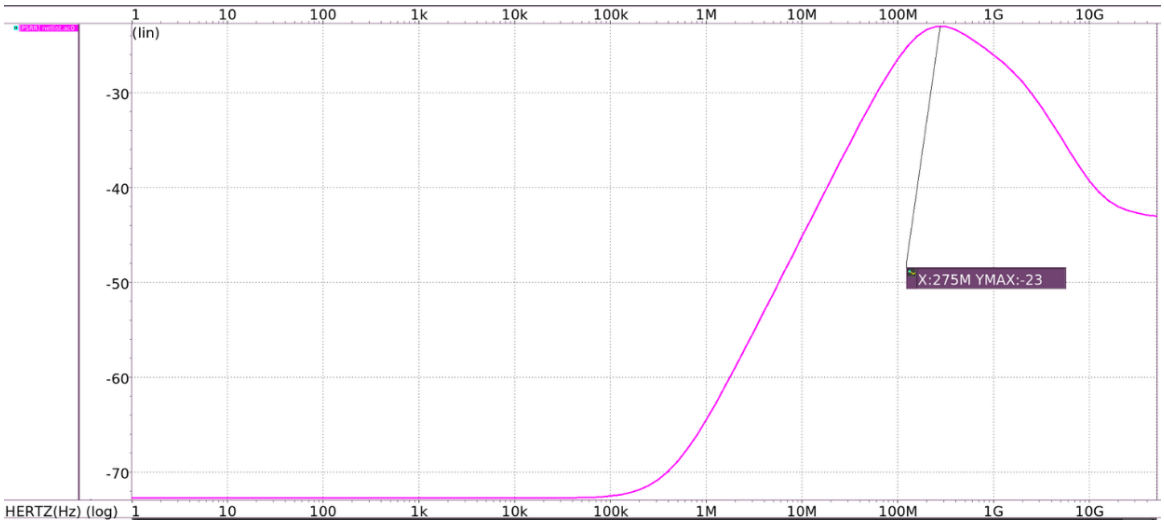
The waveforms for these measurements are shown in Fig. 7 and Fig. 8.

Fig. 7



Amplitude-frequency and phase-frequency plots for Vreg

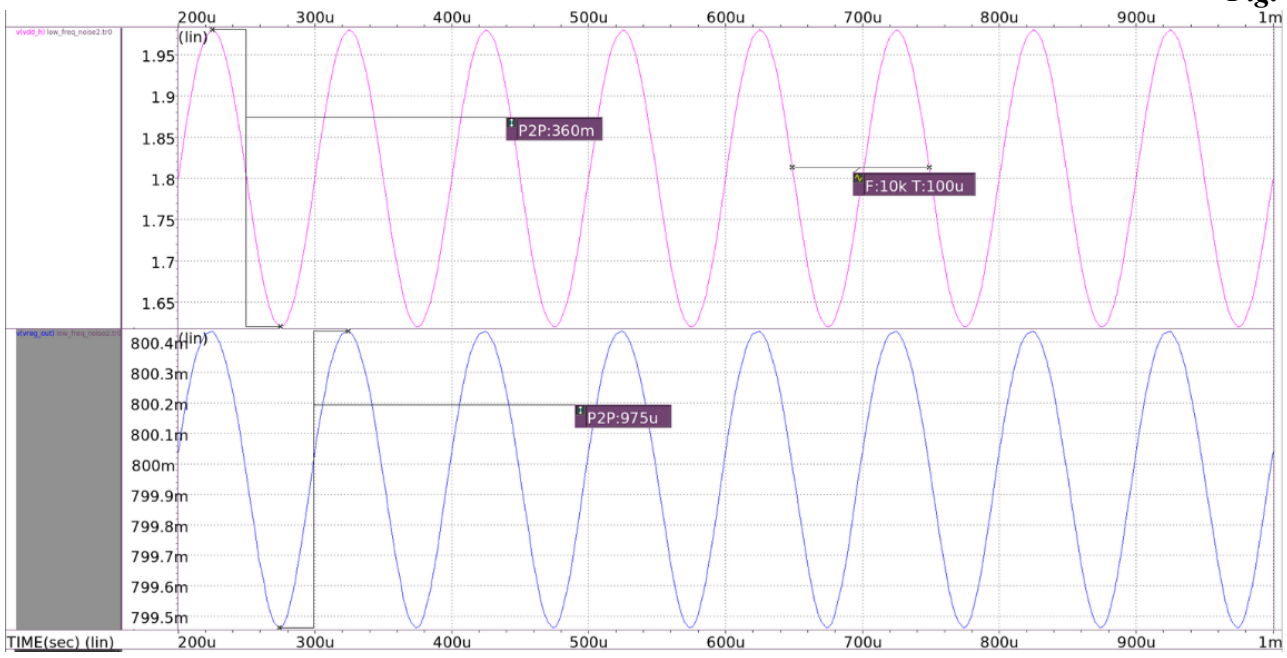
Fig. 8



PSRR plot for Vreg

To evaluate the stability on the RO's output frequency the sinusoidal signal source is connected in series with supply voltage source with amplitude equal its ±10% and with 10kHz frequency. Fig. 9 shows that the change on the output voltage of vreg in this case is less than 1mV.

Fig. 9



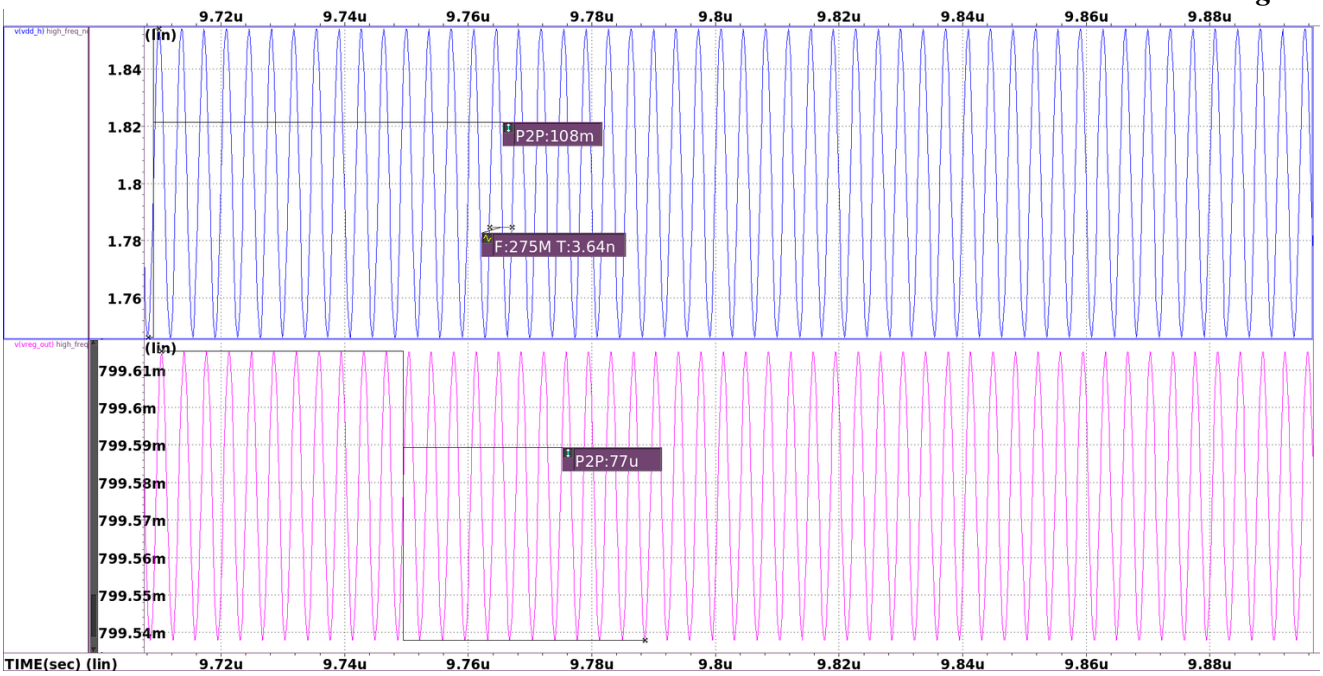
Vreg's output voltage when the supply voltage has low-frequency noise components

This 1mV change forces the RO's output signal to change by ±65MHz which is noticeably better than in the previous case(8-12GHz).

To be sure that the system is working properly also for high frequencies this time the sinusoidal signal source with 275MHz and ±3% amplitude is connected to the supply. The frequency value is chosen based on vreg's PSRR results, where the supply noise suppression is minimal.

As we can see in this case the vreg's output voltage is changing by 77uV thus causing ±23MHz change on RO's output, which is even better than for low frequencies (Fig. 10).

Fig. 10



Vreg's output voltage when the supply voltage has high-frequency noise components

Conclusion

The results are showing that this method is able to provide high frequency stabilization for RO's and this can increase noise immunity for phase-locked loops and can be solution for other problems as well. The proposed solution also has its disadvantages such as big area and need of bipolar transistor usage.

References

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